

changes increase the internal I/O bandwidth by at least a factor of 8. Four internal buses are used to route these internal I/O lines. Increasing the number of I/O lines and then splitting them in the middle greatly reduces the capacitance of each internal I/O line which in turn reduces the column access time, increasing the column access bandwidth even further.

IN THE CLAIMS:

Kindly cancel claims (1-150, without prejudice.

Kindly add the following claims:

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1 ~~151. A synchronous memory device including an array of~~
2 ~~memory cells, the synchronous memory device comprises:~~

3 ~~clock receiver circuitry to receive an external clock signal;~~
4 ~~input receiver circuitry to sample a first operation code~~
5 ~~synchronously with respect to a transition of the external clock~~
6 ~~signal;~~

7 ~~a programmable register to store a value which is representative~~
8 ~~of an amount of time to transpire before the memory device outputs~~
9 ~~data, wherein the memory device stores the value in the programmable~~
10 ~~register in response to the first operation code; and~~

11 ~~output driver circuitry to output data in response to a second~~
12 ~~operation code, wherein the data is output after the amount of time~~
13 ~~transpires, and wherein:~~

14 ~~the output driver circuitry outputs a first portion of the~~
15 ~~data synchronously with respect to a rising edge transition of the~~
16 ~~external clock signal and outputs a second portion of the data~~
17 ~~synchronously with respect to a falling edge transition of the~~
18 ~~external clock signal.~~

1 ~~152. The memory device of claim 151 wherein the first operation~~
2 ~~code is included in a control register access packet.~~

3 ~~153. The memory device of claim 152 wherein the first operation~~
4 ~~code and the value are included in the same control register access~~
5 ~~packet.~~

6 ~~154. The memory device of claim 151 wherein the memory device is~~
7 ~~a synchronous DRAM.~~

8 ~~155. The memory device of claim 151 wherein the input receiver~~
9 ~~circuitry receives the second operation code and address information~~
10 ~~corresponding to at least one memory cell location of the array of~~
11 ~~memory cells.~~

12 ~~156. The memory device of claim 151 wherein the input receiver~~
13 ~~circuitry receives at least one of the second operation code and~~

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address information corresponding to at least one memory cell location of the array of memory cells.

1 157. The memory device of claim 151 wherein the amount of time is
2 representative of a number of clock cycles of the external clock
3 signal.

1 158. The memory device of claim 151 wherein the input receiver
2 circuitry receives a third operation code, wherein the third operation
3 code initiates a write operation in the memory device.

1 159. The memory device of claim 158 wherein the input receiver
2 circuitry receives the third operation code and address information
3 corresponding to at least one memory cell location of the array of
4 memory cells.

1 160. The memory device of claim 151 further including delay lock
2 loop circuitry coupled to the clock receiver circuitry to generate a
3 first internal clock signal, wherein the data is output using the first
4 internal clock signal.

1 161. The memory device of claim 151 wherein the output driver
2 circuitry outputs the data onto a bus.

1 162. The memory device of claim 161 wherein the bus includes a set
2 of signal lines used to transmit multiplexed address information, data
3 and control information.

1 163. A method of operation of a synchronous memory device, wherein
2 the memory device includes an array of memory cells and a programmable
3 register, the method of operation of the memory device comprises:
4 sampling a first operation code synchronously with respect to an
5 external clock signal;
6 receiving a binary value wherein the memory device stores the
7 binary value in the programmable register in response to the first
8 operation code wherein the binary value is representative of an amount

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of time to transpire before the memory device outputs data in response to a second operation code;

11 sampling the second operation code; and

12 outputting data after the amount of time transpires, wherein a
13 first portion of the data is output synchronously with respect to a
14 first transition of the external clock signal and a second portion of
15 the data is output synchronously with respect to a second transition of
16 the external clock signal.

1 164. The method of claim 163 wherein the second operation code is
2 sampled synchronously with respect to the external clock signal.

1 165. The method of claim 163 wherein the binary value is
2 representative of a number of clock cycles of the external clock
3 signal.

166. The method of claim 165 further including:

4 receiving block size information wherein the block size
5 information defines an amount of data to be output in response to the
6 second operation code, wherein the memory device outputs the amount of
7 data after the number of clock cycles of the external clock signal
8 transpire.

2 ~~167. The method of claim 163 further including receiving address
information synchronously with respect to the external clock signal.~~

1 168. The method of claim 163 wherein the address information and
2 the second operation code are included in a read request packet.

1 169. The method of claim 163 further including receiving precharge
2 information.

1 170. The method of claim 169 wherein the precharge information
2 includes a binary bit, wherein, after accessing the data from the array
3 of memory cells, the memory device retains contents of a plurality of

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5C1 sense amplifiers for a subsequent memory operation as a result of a first state of the binary bit.

1 171. The method of claim 163 wherein the first transition of the
2 external clock signal is a rising edge transition and the second
3 transition of the external clock signal is a falling edge transition.

1 172. The method of claim 171 wherein the first and second
2 transitions of the external clock signal are consecutive transitions of
3 the external clock signal.

1 173. The method of claim 163 wherein the first operation code is
2 sampled during an initialization sequence after power is applied to the
3 memory device.

1 174. The method of claim 163 wherein the memory device samples the
2 first operation code from an external bus, and wherein the memory
3 device outputs data onto the external bus.

1 175. The method of claim 174 wherein the external bus includes a
2 set of signal lines used to transmit multiplexed address information,
3 data and control information.

1 176. A method of controlling a synchronous memory device by a
2 memory controller, wherein the memory device includes an array of
3 memory cells and a programmable register, the method of controlling the
4 memory device comprises:

5 issuing a first operation code to the memory device, wherein the
6 first operation code initiates an access of the programmable register
7 in the memory device in order to store a binary value;

8 providing the binary value to the memory device, wherein the
9 memory device stores the binary value in the programmable register in
10 response to the first operation code;

11 issuing a second operation code to the memory device, wherein the
12 second operation code instructs the memory device to accept data that
13 ~~is issued by the memory controller;~~

14 ^{sub}
15 ^{CI} issuing a first portion of the data to the memory device
16 synchronously with respect to a first transition of the external clock
17 signal; and

17 issuing a second portion of the data to the memory device
18 synchronously with respect to a second transition of the external clock
19 signal.

1 177. The method of claim 176 wherein the binary value is
2 representative of a delay time to transpire before the memory device
3 samples the data, and wherein the first portion of the data is issued
4 to the memory device after the delay time transpires.

1 178. The method of claim 176 wherein the binary value is
2 representative of a number of clock cycles of the external clock
3 signal.
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1 179. The method of claim 176 wherein the first transition of the
2 external clock signal is a rising edge transition and the second
3 transition of the external clock signal is a falling edge transition.
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1 180. The method of claim 176 further including:
2 providing block size information to the memory device, wherein the
3 block size information defines an amount of data to be accepted by the
4 memory device in response to the second operation code.

1 181. The method of claim 176 further including providing address
2 information to the memory device.

1 182. The method of claim 181 wherein the address information and
2 the second operation code are included in a write request packet.

1 183. The method of claim 176 wherein the first operation code and
2 the data are issued onto an external bus.

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2 184. The method of claim 183 wherein the external bus includes a
3 set of signal lines used to transmit multiplexed address information,
data and control information.

1 185. The method of claim 176 wherein the second operation code
2 includes precharge information.

1 186. A synchronous memory device, wherein the memory device
2 includes an array of memory cells, the memory device comprises:
3 input receiver circuitry to sample a first operation code
4 synchronously with respect to an external clock signal;

5 a programmable register to store a binary value in response to the
6 first operation code, wherein the binary value is representative of an
7 amount of time to transpire before the memory device outputs data; and

8 output driver circuitry to output data in response to a second
9 operation code and after the amount of time transpires, wherein a first
10 portion of the data is output synchronously with respect to a first
11 transition of the external clock signal and a second portion of the
12 data is output synchronously with respect to a second transition of the
13 external clock signal.

1 187. The memory device of claim 186 wherein the binary value is
2 representative of a number of clock cycles of the external clock
3 signal.

1 188. The memory device of claim 187 wherein the binary value is
2 representative of a fractional number of clock cycles of the external
3 clock signal.

1 189. The memory device of claim 186 wherein the first transition
2 of the external clock signal is a rising edge transition and the second
3 transition of the external clock signal is a falling edge transition.

1 189. The memory device of claim 188 wherein the first and second
2 ~~transitions of the external clock signal are consecutive transitions.~~

1 190. The memory device of claim 189 wherein the first operation
2 code and the binary value are included in a packet.

1 191. The memory device of claim 190 wherein the first operation
2 code and the binary value are included in the same packet.

1 192. The memory device of claim 186 further including delay lock
2 loop circuitry to generate a first internal clock signal, wherein the
3 data is output using the first internal clock signal.

1 193. The memory device of claim 186 wherein the input receiver
2 circuitry receives address information corresponding to at least one
3 memory cell location of the array of memory cells.

1 194. The memory device of claim 186 wherein the output driver
2 circuitry outputs data onto an external bus having a set of signal
3 lines used to transmit multiplexed address information, data and
control information.

1 195. The memory device of claim 194 wherein the input receiver
2 circuitry samples the first operation code from the external bus.

1 196. The memory device of claim 186 wherein the output driver
2 circuitry and the input receiver circuitry are connected to a common
3 pad.

1 197. The memory device of claim 186 wherein the memory device is
2 a synchronous DRAM. --

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